Atty. Docket No. OF03P107/US
Serial No: 10/627,300

Remarks

Applicant and his representatives wish to thank Examiner Malsawma for the thorough examination of the present application, the detailed explanations in the Office Action dated September 9, 2004, and the helpful and courteous discussion held with the undersigned on June 17, 2005, at which U.S. Patent No. 6,562,687 (to Deleonibus et al.) was brought to the attention of the undersigned. Upon further study of the Deleonibus et al. patent, it is believed that Deleonibus et al. do not disclose a short channel transistor, primarily because the gate oxide thickness taught by Deleonibus et al. is necessarily less than the sacrificial oxide layer previously formed in the same location in the transistor. On the other hand, the present invention forms short-channel transistors by ensuring that the gate insulation layer has a thickness sufficient to reach the (second) spacers. The following remarks shall further summarize and expand upon other topics discussed.

Deleonibus et al. discloses an MIS transistor comprising a channel region (118), source (114) and drain (116) regions arranged on either side of the channel, and a gate (150) set closely above the channel region (Abstract, ll. 1-4). Notably, after forming lateral spacers 122, called "interior" spacers, above a channel region, one or several ionic implantation(s) make it possible to adjust the threshold voltage of the transistors by using a coating layer 124 and the lateral spacers 122 as implantation mask (col. 5, ll. 58-65, col. 6, ll. 5-14, and FIG. 5). Thereafter, pedestal layer 102 at the bottom of the well is eliminated by de-oxidation (col. 7, ll. 9-10, and FIG. 7). During this stage one also eliminates a part of the pedestal layer located under the spacers to form a cavity or recess, 142, extending as far as above the source and drain zones 114, 116. At least a part of the oxide layer 134 covering the spacers is also eliminated during de-oxidation, a particularly advantageous characteristic since it encourages the formation of the cavity 142 (col. 7, ll. 14-21, and FIG. 7).

Deleonibus et al. then forms an insulating gate layer 144, which covers the bottom of the well 130 and extends into the cavity 142 (col. 7, ll. 22-24, and FIG. 8). The gate material is then set in place in the well 130, and extends into the cavity 142 so that in cross-section, the gate has the shape of an upside-down T (col. 7, ll. 36-55, and FIG. 9). **Since the gate oxide formed at**

the bottom of the well has a lower thickness than that of the oxide of the pedestal layer, one obtains in fine, a gate with a cross section of an upside-down T (col. 3, ll. 53-56; emphasis added). Thus, by forming a gate oxide having a lower thickness than that of the previously-formed pedestal oxide, and thereby filling in at least part of the cavity 142, gate 150 does not, and cannot, form a short-channel transistor.

In one variant, Deleonibus et al. suggest that one can eliminate only part of the thickness of the pedestal layer at the bottom of the well to avoid formation of the gate insulator layer, but this solution is less advantageous because it does not allow fine control of the thickness of the layer of remaining oxide, and does not encourage production of the cavity 142 (col. 7, ll. 31-35). This suggests the criticality of forming cavity 142, and thus, of making a gate with a cross section of an upside-down T.

In another variant, Deleonibus et al. disclose interior lateral spacers 122 resting against the exterior spacers 120 and against the edge of the coating layer 124, at the level of a discontinuity 121 resulting from the combined effects of a parasitic etching of the coating layer during the elimination (by etching) of the dummy gate and an etching of the upper part of the exterior spacers 120 (in nitride) during elimination of the layer of silicon nitride 106 of the dummy layer (col. 8, ll. 4-5 and 9-24, and FIGS. 10-11). However, the subsequent operations are identical to those described elsewhere by Deleonibus et al. (col. 8, ll. 25-26). This particular variant makes it possible to accentuate the T shape of the part of the definitive gate which will finally be formed in the well. Thus, the gate in this variant has a cross-section shaped in a double T (T and upside-down T), also called an I shape (col. 8, ll. 26-32). As a result, Deleonibus et al. neither discloses nor suggests a method for forming short-channel transistors. In fact, it could very well defeat one or more of the purposes of the technology disclosed by Deleonibus et al. to modify their disclosure in the manner necessary to arrive at the present invention.

In contrast, the present invention relates to a method for forming short-channel transistors. In key steps, the presently claimed process forms a punch-stop layer on the substrate by ion implantation between second spacers and through a first oxide layer in an opening from

which a residual sacrificial layer pattern was removed, then ensures formation of short-channel transistors by forming a gate insulation layer having a thickness sufficient to reach the second spacers. (Prior to removal of a residual sacrificial layer pattern, first spacers are on its sidewalls, an LDD ion-implant layer is in the semiconductor substrate at a location not masked by the residual sacrificial layer pattern, and a source/drain ion-implant layer is under the LDD ion-implant layer at a location not masked by the first spacers.) After forming the punch-stop layer, the first oxide layer is removed, the gate insulation layer having a thickness sufficient to reach the second spacers is formed, and a gate is formed on the gate insulation layer and the second spacers.

The primary reference cited against the originally-filed claims (Woerlee et al., U.S. Pat. No. 6,406,963 [hereinafter "Woerlee"]) neither discloses nor suggests ion implanting a punch stop layer between second spacers and through a first oxide layer that is subsequently removed. Thus, Woerlee cannot suggest forming a gate on such second spacers. Furthermore, because Woerlee does not form second spacers prior to ion implanting a punch stop layer, Woerlee does not and cannot disclose or suggest forming a gate insulation layer having a thickness sufficient to reach the second spacers.

The secondary references cited against the claims (Wu, U.S. Pat. No. 5,856,226 [hereinafter "Wu '226"] and Yu et al., U.S. Pat. No. 6,180,468 [hereinafter "Yu et al. '468"]) fail to cure all of the salient deficiencies of Woerlee, and the references taken as a whole fail to provide sufficient reasons, motivation or suggestions to combine their disclosures in the manner necessary to arrive at the present invention (i.e., to make the combination of forming a punch stop implant layer through spacers in a substrate that already has LDD and source/drain implant layers therein), at least not without the benefit of the hindsight provided by the present application. Consequently, the present claims are patentable over the cited references.

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The Rejection of Claims 1-5, 7, 11-16 and 19-20 under 35 U.S.C. § 103(a)

The rejection of Claims 1-5, 7, 11-16 and 19-20 under 35 U.S.C. § 103(a) as being unpatentable over Woerlee in view of Wu '226 is respectfully traversed.

Woerlee discloses a method of manufacturing a semiconductor device (Abstract, l. 1). The surface 2 of the semiconductor body 1 is provided with a layer 7 composed of, for example, silicon oxide, which is covered by a patterned layer 10 defining the area of a gate structure to be provided in a later stage of the process (col. 5, ll. 31-35, and FIG. 1). After applying the patterned layer 10, source/drain extensions 11 are formed on opposite sides of the patterned layer 10 by means of a self-aligned implantation of a relatively light dose of, for example, phosphorus or arsenic, using the patterned layer 10 together with the oxide field insulating regions 3 as a mask (col. 5, ll. 55-60, and FIG. 1). Subsequently, the patterned layer 10 is provided with sidewall spacers 13 (col. 5, ll. 64-67, and FIG. 2). After formation of the sidewall spacers 13, a highly-doped source zone 14 and a highly-doped drain zone 15 are formed on opposite sides of the sidewall spacers 13 by means of a self-aligned implantation of a heavier dose of, for example, phosphorus or arsenic, using the oxide field insulating regions 3 together with the patterned layer 10 and the sidewall spacers 13 as a mask (col. 5, l. 67 through col. 6, l. 7, and FIG. 2).

An etch stop layer 17 and a relatively thick dielectric layer 18 are applied in such a way that the thickness of the dielectric layer 18 next to the patterned layer 10 is substantially equally large or larger than the height of the patterned layer 10 (col. 6, ll. 12-19, and FIG. 3). Subsequently, the dielectric layer 18 is removed, for example, by chemical-mechanical polishing (CMP) over part of its thickness until the patterned layer 10 is exposed (col. 6, ll. 26-30, and FIG. 4). During the CMP treatment, the second sub-layer 9 will act as a stop layer (col. 6, ll. 30-32).

In a next step (FIG. 5), the second sub-layer 9 is removed selectively with respect to the dielectric layer 18 and the sidewall spacers 13, providing the dielectric layer 18 with a recess 19 in which the first sub-layer 8 is exposed (col. 6, ll. 33-42). Thereafter, the first sub-layer 8 and the layer 7 are removed in two separate etching steps, although the layer 7 may be preserved in

the recess 19 and used as a gate dielectric of the transistor (col. 6, ll. 43-52; see also col. 10, ll. 3-6). The semiconductor body 1 is then provided with an impurity region 20 via the recess 19 at the area of the gate structure 21 into the semiconductor body 1 in a self-registered way by using the dielectric layer 18 as a mask. The impurity region 20 can be applied as a shallow region to suppress short-channel threshold-voltage reduction and/or a deeper region to suppress punch-through between the extended source zone 14,11 and the extended drain zone 15,11 (col. 6, ll. 53-63; see also col. 10, ll. 6-21).

Woerlee does not disclose or suggest ion implanting a punch stop layer between second spacers in a recess from which a residual sacrificial layer pattern (e.g., patterned layer 10) was removed. To the extent that Woerlee suggests implanting a punch stop layer through an oxide layer (see, e.g., col. 5, ll. 31-35, and col. 7, ll. 37-44), Woerlee teaches that such an oxide layer is used as the gate dielectric of the transistor (col. 6, ll. 50-52), and that, if it has a high dielectric constant, the high-temperature anneal associated with the punch stop ion implantation may degrade its dielectric properties (col. 7, ll. 44-49). Thus, Woerlee neither discloses nor suggests ion implanting a punch stop layer between second spacers and through a first oxide layer that is subsequently removed. As a necessary consequence, Woerlee cannot suggest forming a gate on second spacers that were formed where a residual sacrificial layer pattern was removed.

Furthermore, Woerlee does not form second spacers prior to ion implanting a punch stop layer. As a result, Woerlee does not and cannot disclose or suggest forming a gate insulation layer having a thickness sufficient to reach the second spacers. Thus, Woerlee is saliently deficient with regard to the presently claimed invention.

Wu '226 fails to cure the salient deficiencies of Woerlee with regard to the presently claimed invention. Although Wu '226 teaches forming a punchthrough stopping implant region 24 between first spacer structures 20 on the side wall of a hollow space 18 over a thin silicon oxide layer 12 by doping (like an ion implantation process; see col. 5, ll. 48-51 and 63-65, and FIG. 2), Wu '226 does not disclose, teach or suggest that such a punchthrough stopping implant region can be formed in a structure that already has spacers that were formed on side walls of a sacrificial layer pattern that was removed to form the "hollow space," an LDD ion-implant layer

in the semiconductor substrate (at a location not masked by the sacrificial layer pattern), and a source/drain ion-implant layer under the LDD ion-implant layer (at a location not masked by the previously formed spacers). For example, Wu '226 forms the LDD ion-implant layer 46 **after** forming punchthrough stopping implant region 24 and source/drain implant layers 42 (see, e.g., FIGS. 12-14 and col. 7, l. 55-col. 8, l. 38).

There must be some reason, suggestion, or motivation found in the prior art whereby a person of ordinary skill in the field of the invention would make a claimed combination. That knowledge cannot come from the applicant's invention itself. *In re Oetiker*, 977 F.2d 1443, 1447; 24 U.S.P.Q.2d 1443 (Fed. Cir. 1992); citing *Diversitech Corp. v. Century Steps, Inc.*, 850 F.2d 675, 678-79, 7 USPQ2d 1315, 1318 (Fed. Cir. 1988); *In re Geiger*, 815 F.2d 686, 687, 2 USPQ2d 1276, 1278 (Fed. Cir. 1987); *Interconnect Planning Corp. v. Feil*, 774 F.2d 1132, 1147, 227 U.S.P.Q. 543, 551 (Fed. Cir. 1985). In this case, Woerlee does not provide any reason, suggestion or motivation to form a punch stop implant layer through spacers as taught by Wu '226, nor does Wu '226 provide any reason, suggestion or motivation to form a punch stop implant layer by ion implantation between spacers in a substrate that already has LDD and source/drain implant layers therein. Thus, the cited references fail to provide any reason, suggestion, or motivation by which a person of ordinary skill in the field of the invention would make the combination of forming a punch stop implant layer through spacers in a substrate that already has LDD and source/drain implant layers therein, as presently claimed. Therefore, this ground of rejection is legally unsustainable, and should be withdrawn.

Similar to the discussion in the Amendment filed January 5, 2005, there may be reasons understood by those of ordinary skill in the art not to modify a process that forms a channel implant in a substrate that already has LDD and source/drain implant layers therein with steps from a process that forms LDD and source/drain implant layers after forming a punch stop implant layer. For example, ion implants generally require annealing for substrate crystal lattice repair and dopant activation (see, e.g., Wolf et al., "Silicon Processing for the VLSI Era," vol. 1 (2000), pp. 386-398, submitted with the Amendment filed January 5, 2005). However, annealing generally results in diffusion (i.e., migration) of dopant atoms by a complex process made even

more complex by implantation damage (Wolf et al., pp. 396-7). Punch stop implants are known to be somewhat sensitive to a variety of factors, including implant depth, implant dose, applied electric field, and channel length (see, e.g., Wolf, "Silicon Processing for the VLSI Era," vol. 2 (1990), pp. 341-7, submitted with the Amendment filed January 5, 2005). Source/drain implants generally require a "drive-in" annealing step that shortens the effective channel length due to lateral diffusion of implanted dopant atoms (see Wolf, vol. 2, pp. 333-4). Thus, one of ordinary skill in the art might be motivated **not** to modify a process that forms a channel implant in a substrate that already has LDD and source/drain implant layers therein with steps from a process that forms LDD and source/drain implant layers *after* forming a punch stop implant layer, because there could be reasonable uncertainty about the potential migration or diffusion of the other implant-based structures.

This is not to say that the Examiner's position as set forth on p. 9 of the Office Action dated March 21, 2005 is completely wrong or without merit. However, the source/drain implants and LDD structures of Wu '226 are formed at a different time than in the process Woerlee. As a result, based on the evidence in the record, it would appear that one can conclude that one of ordinary skill in the art would modify the structure and method of Woerlee by carefully picking and choosing certain structural elements and processing steps disclosed by Wu '226, and ignoring others, in order to arrive at the present claims and obtain the benefits of the claimed invention, only if one has the benefit of the hindsight created by the present application.

One of ordinary skill may understand, for example, that Woerlee teaches formation of a relatively wide channel implant, due to the absence of spacers in the channel implant recess 19, perhaps because the LDD implants 11 and source/drain implants 14/15 are already formed (and quite possibly annealed) by the time channel impurity region 20 is formed. Also, one of ordinary skill may also understand Wu '226 to teach a relatively wide punchthrough stopping implant region 24, even though the implant occurs between first spacer structures 20 in hollow space 18, because the subsequent formation of source/drain implants 42 and LDD implants 46 require extensive annealing (col. 8, ll. 7-13 and 44-48 of Wu '226) that may cause the atoms in punchthrough stopping implant 24 to diffuse, or migrate, a relatively long distance in comparison

to the atoms in channel impurity region 20 of Woerlee. Neither reference appears to disclose, teach, or suggest taking any further steps to reduce or minimize the width of the ion-implanted regions in the transistor channel. As a result, one of ordinary skill in the art might not understand the cited references to suggest forming a punch stop implant layer through spacers in a substrate that already has LDD and source/drain implant layers therein, as a way to reduce the or minimize the width of the ion-implanted regions in the transistor channel even further than the disclosure of Wu '226.

To assert that one of ordinary skill in the art would understand the benefits of the invention as a result of modifying the disclosures of the cited references in the manner necessary to arrive at the invention, without any suggestion in the references to do so, is a classic hindsight reconstruction of the invention. One cannot use hindsight reconstruction to pick and choose among isolated disclosures in the cited references to deprecate the claimed invention. *In re* Fine, 837 F.2d 1071, 1075, 5 U.S.P.Q.2d 1596, 1600 (Fed. Cir. 1988); see also *In re* Pleudemann, 910 F.2d 823, 828, 15 U.S.P.Q.2d 1738, 1742 (Fed. Cir. 1990); and *Uniroyal, Inc. v. Rudkin-Wiley Corp.*, 837 F.2d 1044, 1051, 5 U.S.P.Q.2d 1434, 1438 (Fed. Cir. 1988). To use the patent [application] as a guide through the cited references, combining the right disclosures in the right way to arrive at the result of the claimed invention, is improper. See, e.g., *Medtronic, Inc. v. Daig Corp.*, 611 F. Supp. 1498, 1534, 227 U.S.P.Q. 509, 535 (D. Minn. 1985), *aff'd* 789 F.2d 903, 229 U.S.P.Q. 664 (Fed. Cir. 1986).

As a result, the cited references fail to provide any reason, suggestion, or motivation by which a person of ordinary skill in the field of the invention would make the combination of forming a punch stop implant layer through spacers in a substrate that already has LDD and source/drain implant layers therein, at least not without the benefit of the hindsight provided by the present application. Therefore, this ground of rejection is unsustainable, and should be withdrawn.

The Rejection of Claims 6, 8-10, 17 and 18 under 35 U.S.C. § 103

The rejection of Claims 6, 8-10, 17 and 18 under 35 U.S.C. § 103(a) as being unpatentable over Woerlee in view of Yu et al. '468 is respectfully traversed.

As discussed above, Woerlee fails to disclose, teach or suggest ion implanting a punch stop layer between second spacers in a recess from which a residual sacrificial layer pattern was removed. As a necessary consequence, Woerlee cannot suggest forming a gate on second spacers that were formed where a residual sacrificial layer pattern was removed. Furthermore, Woerlee does not form second spacers prior to ion implanting a punch stop layer. As a result, Woerlee does not and cannot disclose or suggest forming a gate insulation layer having a thickness sufficient to reach the second spacers. Yu '468 fails to cure the salient deficiencies of Woerlee with regard to the presently claimed invention.

Yu et al. '468 discloses an ultra-low thermal budget process for channel implant by using a reverse process sequence (Abstract, ll. 1-4). The originally deposited polysilicon gate is removed, a nitride film deposition and etch is used to form a nitride spacer, and a self-aligned channel implant is performed. After the channel implantation, anneal and super-retrograded doping, the nitride spacer and the gate oxide are removed for subsequent regrowth of a second gate oxide and a polysilicon deposition to form a second polysilicon gate (Abstract, ll. 4-11).

More specifically, Yu et al. '468 discloses filling the void where the polysilicon gate 24 was etched away with a nitride deposition (col. 3, ll. 30-32, and FIG. 4). The nitride deposition is then etched down to the gate oxide 22 to form nitride gate spacers 32 and 34 (col. 3, ll. 32-34, and FIG. 4). After the nitride gate spacers 32 and 34 are formed, a dopant implantation 36 is made through the gate oxide 22 into the silicon substrate 12 to form a doped area 38 (col. 3, ll. 32-34, and FIG. 4). The nitride gate spacers 32 and 34, and the gate oxide 22 are then removed (col. 3, ll. 42-44, and FIG. 5). After an anneal, the channel dopant will have a super-retrograded doping profile (col. 3, ll. 44-47). A second gate oxide 40 is regrown on the silicon substrate 12, and a second polysilicon gate 42 is deposited on top of the second gate oxide 40 (col. 3, ll. 64-67, and FIG. 6). Finally, chemical-mechanical polishing is used to level the polysilicon gate with the oxide 30 to form the final MOS transistor 44 (col. 3, l. 67, through col. 4, l. 2, and FIG. 6).

Yu et al. '468 is silent with regard to forming a gate on second spacers that were formed where a residual sacrificial layer pattern was removed. Consequently, Yu et al. '468 does not and cannot disclose or suggest forming a gate insulation layer having a thickness sufficient to reach the second spacers. As a result, neither reference, either alone or taken in combination, can possibly disclose or suggest this aspect of the presently claimed invention. Thus, Yu et al. '468 cannot cure the salient deficiencies of Woerlee with regard to the present claims.

Consequently, this ground of rejection is unsustainable, and should be withdrawn.

The Objections to Claims 9 and 20

The objection to Claim 9 is respectfully traversed.

As filed on January 5, 2005, the previous Amendment amended "nitride layers" to --a nitride layer--, in part by striking through the "s" in the word "layers" (see p. 5 of the Amendment filed January 5, 2005, in which the struck-through "s" is circled). Applicant's undersigned representative regrets any inconvenience or confusion caused, to the extent this particular amendment was not readily apparent.

The objection to Claim 20 has been overcome by appropriate amendment.

Conclusions

In view of the above amendments and remarks, all bases for objection and rejection are believed to be overcome, and the application is believed to be in condition for allowance. Early notice to that effect is earnestly requested.

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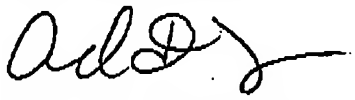
If it is deemed helpful or beneficial to the efficient prosecution of the present application, the Examiner is invited to contact Applicant's undersigned representative by telephone.

Respectfully submitted,



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